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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,490	12/04/2003	Zi-Ping Chen	681954-45U1	7535

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EXAMINER	
BAUER, SCOTT ALLEN	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,490	CHEN ET AL.	
	Examiner	Art Unit	
	Scott Bauer	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/05/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 8 & 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Lai et al. (US 2002/0089017).

With regard to Claim 8, Lai et al., in Figures 4 & 7, discloses an integrated circuit for electrostatic discharge (ESD) protection comprising: a silicon-controlled rectifier (104); a p-type transistor (180) formed integrally with the SCR; an n-type transistor (178) formed integrally with the SCR; a control circuit (244 & 250) coupled to the p-type and n-type transistors providing a first holding voltage to the SCR to keep the SCR from latching-up, and providing a second holding voltage to the SCR to keep the SCR in the latch-up state (paragraph 0057).

With regard to Claim 9, Lai et al., in Figure 7, discloses the circuit of claim 8, the control circuit further comprising a resistor (244), a capacitor (250) and an output terminal (A) disposed between the resistor and the capacitor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-15 & 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6,309,940) in view of Lai et al. (US 2002/0089017).

With regard to Claim 1, Lee teaches an integrated circuit comprising: a silicon-controlled rectifier (column 1 lines 20-25); a first transistor (27, 28) of a first type (P-channel FET) integrally formed with the SCR including a first gate (37); a second transistor (25, 26) of a second type (N-channel FET) integrally formed with the SCR including a second gate (38); and a control circuit (V_{in}) which provides a first and second voltage to the first and second gates (37 & 38).

Lee does not teach that the control circuit provides a first holding voltage to the SCR to keep the SCR from latching-up, and in response to a second voltage applied to the first and second gates providing a second holding voltage to the SCR to keep the SCR in the latch-up state.

Lai et al., in Figures 7 A&B, teaches an SCR device used to protect an I/O pad wherein a control circuit is coupled to first and second gates of N and P type FETs and that by driving the gates, the control circuit provides a first holding voltage to the SCR to keep the SCR from latching-up, and in response to a second voltage applied to the first and second gates providing a second holding voltage to the SCR to keep the SCR in the latch-up state (paragraph 0057).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lee with Lai et al., by coupling the control circuit (244 & 250) taught by Lai et al., at node A, to the control signal (V_{in}) of Lee, for the purpose of avoiding latch-up while the SCR operates at normal condition, but allows for easy triggering of the device in an ESD event (Lai et al. Paragraph 0021).

The integrated circuit taught in Fig. 1 of Lee, is capable of use for electrostatic discharge protection.

With regard to Claims 2-4, Lee in view of Lai et al. discloses the circuit of Claim 1. Lai et al. further discloses that the control circuit further comprises an output terminal (A) coupled to first and second gates. Lai et al. further teaches that the control circuit comprises a resistor (244), a capacitor (250) and an output terminal (A) disposed between the resistor and the capacitor, which provides a resistor-capacitor delay circuit.

With regard to Claims 5-7, Lee in view of Lai et al. discloses the circuit of Claim 1. Lee further discloses that the SCR further comprising a p-type substrate (11), an n-well (21) formed in the p-type substrate, a p-type diffused region (28) formed in the n-well, and an n-type diffused region (25) formed outside of the n-well. Lee further teaches that the first transistor further comprises a channel region formed in the n-well and that the second transistor further comprises a channel region formed in the p-type substrate (column 1 lines 40-44, 55-59).

With regard to Claim 8, Lee teaches an integrated circuit for electrostatic discharge (ESD) protection comprising: a silicon-controlled rectifier (SCR); a p-type transistor formed integrally with the SCR; an n-type transistor formed integrally with the SCR; a control circuit coupled to the p-type and n-type transistors.

Lee does not teach that the control circuit provides a first holding voltage to the SCR to keep the SCR from latching-up, or provides a second holding voltage to the SCR to keep the SCR in the latch-up state.

Lai et al., in Figures 7 A&B, teaches an SCR device used to protect an I/O pad wherein a control circuit is coupled to first and second gates of N and P type FETs and that by driving the gates, the control circuit provides a first holding voltage to the SCR to keep the SCR from latching-up, and in response to a second voltage applied to the first and second gates providing a second holding voltage to the SCR to keep the SCR in the latch-up state (paragraph 0057).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lee with Lai et al., by coupling the control circuit (244 & 250) taught by Lai et al., at node A, to the control signal (V_{in}) of Lee, for the purpose of avoiding latch-up while the SCR operates at normal condition, but allows for easy triggering of the device in an ESD event (Lai et al. Paragraph 0021).

The integrated circuit taught in Fig. 1 of Lee, is capable of use for electrostatic discharge protection.

With regard to Claim 9, Lee in view of Lai et al. discloses the circuit of Claim 8. Lai et al. further discloses that the control circuit further comprises a resistor (244), a capacitor (250) and an output terminal (A) disposed between the resistor and the capacitor.

With regard to Claim 10, Lee in view of Lai et al. discloses the circuit of Claim 8. Lai et al., in figure 7A, further discloses that the control circuit comprises an output terminal (A) coupled to a gate of a p-type transistor and a gate of an n-type transistor.

With regard to Claim 11, Lee in view of Lai et al. discloses the circuit of Claim 8. Lee further discloses that the SCR further comprises a first p-type substrate (11), an n-well (21) formed in the p-type substrate, a p-type diffused region (28) formed in the n-well, and a first n-type diffused region (25) formed outside of the n-well.

With regard to Claim 12, Lee in view of Lai et al. discloses the circuit of Claim 11. Lee further discloses that the SCR further comprises a second p-type diffused region (27) partially formed in the n-well (21) to serve as a drain of the p-type transistor, wherein the first p-type diffused region serves as a source of the p-type transistor.

With regard to Claim 13, Lee in view of Lai et al. discloses the circuit of Claim 11. Lee further discloses that the SCR further comprising a second n-type diffused region (26) formed in the p-substrate to serve as a drain of the n-type transistor, wherein the n-type diffused region serves as a source of the n-type transistor.

With regard to Claim 14, Lee in view of Lai et al. discloses the circuit of Claim 8.

Lee teaches that the SCR is coupled between different voltage lines. Lee does not teach that the SCR is coupled between a contact pad and a voltage line.

Lai et al. In Fig. 4 further discloses that the SCR is coupled between a contact pad (100) and a voltage line (GND).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to place the SCR between a contact pad and voltage line instead of two different voltage lines for the purpose of protecting an internal circuit from an ESD event originating at a contact pad.

With regard to Claim 15, Lee in view of Lai et al. discloses the circuit of Claim 8. Lee et al. Further teaches that the SCR is coupled between different voltage lines (VDD & VSS).

With regard to Claim 23, Lee teaches a method of electrostatic discharge protection comprising: providing a silicon-controlled rectifier (SCR) having a holding voltage; integrally forming a first transistor (27 & 28) of a first type with the SCR including a first gate (37); integrally forming a second transistor (25 & 26) of a second type with the SCR including a second gate (38).

Lee does not teach providing a first signal to the first and second gates to raise the holding voltage of the SCR to keep the SCR from latching up; and providing a second signal to the first and second gates to lower the holding voltage of the SCR to keep the SCR in the latch-up state.

Lai et al., in Figures 7 A&B, teaches an SCR device used to protect an I/O pad wherein a control circuit is coupled to first and second gates of N and P type FETs and

that by driving the gates, the control circuit provides a first holding voltage to the SCR to keep the SCR from latching-up, and in response to a second voltage applied to the first and second gates providing a second holding voltage to the SCR to keep the SCR in the latch-up state (paragraph 0057).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lee with Lai et al., by coupling the control circuit (244 & 250) taught by Lai et al., at node A, to the control signal (V_{in}) of Lee, for the purpose of avoiding latch-up while the SCR operates at normal condition, but allows for easy triggering of the device in an ESD event (Lai et al. Paragraph 0021).

The integrated circuit taught in Fig. 1 of Lee, is capable of use for electrostatic discharge protection.

1. With regard to Claims 24 & 25, Lee in view of Lai et al. discloses the method of Claim 23. Lai et al. further discloses that the method further comprises raising the holding voltage of the SCR to above a power supply voltage and lowering the holding voltage of the SCR to below a power supply voltage (Lai et al. Paragraph 0057).

With regard to Claim 26, Lee in view of Lai et al. discloses the circuit of Claim 23.

Lee teaches that the SCR is coupled between different voltage lines. Lee does not teach that the SCR is coupled between a contact pad and a voltage line.

Lai et al. In Fig. 4 further discloses that the SCR is coupled between a contact pad (100) and a voltage line (GND).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to place the SCR between a contact pad and voltage line instead of two different voltage lines for the purpose of protecting an internal circuit from an ESD event originating at a contact pad.

With regard to Claim 27, Lee in view of Lai et al. discloses the circuit of Claim 8. Lee et al. Further teaches that the SCR is coupled between different voltage lines (VDD & VSS).

2. Claims 16-22 & 28-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. In view of Lai et al. as applied to claims 1, 8 & 23 above, and further in view of Tong et al. (US 6,756,834).

With regard to Claims 16 & 28, Lee teaches an integrated circuit and a method comprising: a first voltage line (VDD) of a first voltage level; a second voltage line (VSS) of a second voltage level; a silicon-controlled rectifier(SCR), including a p-type transistor and an n-type transistor integrally formed with the SCR.

Lee et al. does not teach a control circuit providing a first holding voltage through the p-type and n-type transistors to the SCR to keep the SCR from latching-up, and providing a second holding voltage through the p-type and n-type transistors to the SCRs to keep the SCRs in the latch-up state during an ESD event that an ESD pulse

appears on the first voltage line or one of the contact pads. Further, Lee does not teach providing a plurality of contact pads or that there is a plurality of SCRs.

Lai et al., in Figures 7 A&B, teaches an SCR device used to protect an I/O pad wherein a control circuit is coupled to first and second gates of N and P type FETs and that by driving the gates, the control circuit provides a first holding voltage to the SCR to keep the SCR from latching-up, and in response to a second voltage applied to the first and second gates providing a second holding voltage to the SCR to keep the SCR in the latch-up state (paragraph 0057).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lee with Lai et al., by coupling the control circuit (244 & 250) taught by Lai et al., at node A, to the control signal (V_{in}) of Lee, for the purpose of avoiding latch-up while the SCR operates at normal condition, but allows for easy triggering of the device in an ESD event (Lai et al. Paragraph 0021).

The integrated circuit taught in Fig. 1 of Lee, is capable of use for electrostatic discharge protection.

Tong et al., in figure 1, discloses an ESD protection circuit comprising a plurality of pads, first and second voltage sources of first and second voltage levels, and a plurality of ESD protection circuits (10 & 14). Tong et al. further teaches that each ESD protection device contains a control circuit comprising a capacitor (16) and a resistor (18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings Lee with Tong et al. by protecting a

plurality of I/O pads and voltage lines with the SCR device taught by Lee for the purpose of providing ESD protection to an entire chip assembly instead of just a single voltage source.

With regard to Claim 17 & 29, Lee in view of Lai et al. and further in view of Tong et al. discloses the circuit of Claim 16 and the method of Claim 28. Tong et al. further discloses that an ESD device (14) is coupled between the first and second voltage lines (VCC & VSS) and that the remaining ESDs are each coupled between a corresponding contact pad and the second voltage line.

With regard to Claim 18 & 30, Lee in view of Lai et al. and further in view of Tong et al. discloses the circuit of Claim 17 and the method of Claim 29. Tong et al. further discloses, in Figure 1, that the ESD pulse is discharged from one of the contact pads (VCC PAD 1) via a voltage line (VCC1) to voltage line (VSS 1). This event is depicted by PATH_B in Figure 1.

With regard to Claims 19 & 31 Lee in view of Lai et al. and further in view of Tong et al. discloses the circuit of Claim 17 and the method of Claim 29. Tong et al., in Figure 1, further discloses that an ESD pulse is discharged from the first voltage (VCC 1) line via the second voltage (20) line to one of the contact pads (VSS PAD 1) via PATH_A.

With regard to Claim 20 & 32, Lee in view of Lai et al. and further in view of Tong et al. discloses the circuit of Claim 17 and the method of Claim 29. Tong et al., in Figure 1, further discloses that an ESD pulse is discharged from one of the contact pads (VCC PAD 1) via the second voltage line (20) to a different contact pad (VSS PAD 1) via PATH_A.

With regard to Claim 21, Lee in view of Lai et al. and further in view of Tong et al. discloses the circuit of Claim 16. Lai et al. further discloses that the control circuit comprises a resistor-capacitor delay circuit.

With regard to Claim 22, Lee in view of Lai et al. and further in view of Tong et al. discloses the circuit of Claim 16. Lai et al. further discloses that the control circuit further comprises an output terminal (A) coupled to a gate of each of the p-type and n-type transistors.

Response to Arguments

The objection to Claims 11-13 & 26 has been withdrawn in light of the corrections of the minor informalities.

Applicant's arguments with respect to claims 1-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Bauer whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SAB
6 JUN 06

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PRIMARY EXAMINER